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Traffic Light Control System

Likai Ye

Xihua University, Chengdu, Sichuan, China

Abstract: ***The traffic light control system is a key component of urban traffic management, and its performance directly impacts the smooth flow of traffic and traffic safety. Based on some issues existing in the current traffic signal control systems, this paper proposes a novel traffic light control system based on intelligent algorithms. This system combines artificial intelligence technology with traditional traffic signal control methods to achieve intelligent control of traffic signals, thereby enhancing traffic efficiency and road safety. The paper provides a detailed explanation of the system's design principles, algorithm implementation, and experimental results. Comparative experiments demonstrate that the system has significant advantages in reducing traffic congestion and improving vehicle passage efficiency. Finally, the paper discusses possible future improvement directions and application scenarios, envisioning the development prospects of traffic light control systems in the future.***

Keywords: Traffic control system; Traffic safety.

1. INTRODUCTION

1.1 Purpose and significance of the selection of the topic

Hardware circuits such as 8086 CPU chip as well as 8255A chip and LEDs were utilised for the design of traffic light control. Software design and write the source programme. Traffic in people's daily life occupies an important position, with the increasing frequency of people's social activities, this point is more fully embodied. The emergence of traffic signals, so that traffic can be effectively controlled, for the diversion of traffic flow, improve road capacity, reduce traffic accidents have obvious effects. This system uses 8086 as the central device to design the traffic light controller, the system is practical, easy to operate, strong expansion. This design is the use of 8086 minimum mode in Protues7.8SP2 software to simulate the intersection of traffic lights in a variety of state display. This design system consists of 8255AI/O port expansion system, traffic light status display system, LED display system and other major components. The system implements the functions of traffic light display, emergency handling, etc., and better simulates and realises the possible conditions of the intersection. This system is written in 8086 assembly language, and the main program is mainly written, and the software is generally completed.

1.2 Design objectives

(1) Consolidate and deepen the knowledge learnt in the classroom.

(2) Learning to master the general hardware and software design methodology and the ability to access and use information.

(3) Through the control of traffic lights design and production, in-depth understanding and master the use of programmable 8255A switching control principles and methods.

(4) Master the basic assembly language syntax writing, learn to use proteus simulation use.

(5) Mastery of the ability to analyse and deal with problems has been enhanced, and the ability to solve problems in actual projects.

1.3 Design Tasks and Requirements

Design an ordinary intersection, the control of traffic lights can be divided into east-west and north-south two groups, each group can be used to red, yellow and green lights are used for traffic management, so the main point of the task is to control the sixteen traffic lights.

Due to hardware resource allocation, we use a set of red lights with a set of green lights to represent the east-west, south-north and yellow lights.

1.3.1 Functional requirements

At intersections traffic signals are east-west and north-south. The signals are controlled by the ABC port of the 8255A.

The pattern of traffic lights coming on and going off is as follows:

Daylight mode:

(1) Passing in the east-west direction and stopping in the north-south direction. That means the green light is on in the east-west direction and the red light is on in the north-south direction. At the same time, the digital tube starts counting down from 9-0 display.

(2) Passage in the east-west direction, stop the passage in the north-south direction. When the digital tube number becomes 3, the green light in the east-west direction goes out, and the yellow light in the east-west direction starts to flash until the digital tube number shows 0, that is, the yellow light stops flashing.

(3) Stop traffic in the east-west direction and pass in the north-south direction. That means the red light is on in the east-west direction and the green light is on in the north-south direction. At the same time, the digital tube starts counting down from 9-0 display.

(4) Stop passing in the east-west direction and pass in the north-south direction. When the digital tube number becomes 3, the green light in the north-south direction goes out, and the yellow light in the north-south direction starts to flash until the digital tube number shows 0, i.e. the yellow light stops flashing.

(5) The above action is cycled 8 times and the traffic light enters the night mode.

Night mode:

(1) The digital display turns off, and the red and green lights in the east-west and north-south directions all go out.

(2) All yellow lights in the east, west, south, and north directions flash at the same time.

(3) Night Mode Cycle 4 times into Day Mode

1.3.2 Specific requirements

Course design report writing format requirements, the details are as follows:

(1) Design Tasks and Requirements

(2) General Programme and Description

(3)Hardware schematic diagram and description

(4) Experimental circuit diagram and description

(5) Flowchart of the main software modules

(6) Source programme list and comments

(7) Proteus simulation (simulation results and related documents)

(8) Problem analysis and solutions (including tuning records, tuning reports, that is, in the process of tuning the main encountered) (Problems, solutions and ideas for improvement)
(9) Summary and experience: Completion part: In this course design mainly complete the design of the software.

Appendix: (1) Source programme (must have simple comments) and component list; (2) Instructions for use; (3) References

2. OVERALL PROGRAMME DESIGN AND DESCRIPTION

2.1 Overall system design programme

This design is based on the TDX-PITE_80X86 in which the design of the hardware circuits, the writing of the assembly language source programme and the debugging of the software system after the completion of the above two parts of the work are carried out.

The processing control system of this design consists of a uniprocessor system composed of Intel 8086 microprocessor in minimal mode, which is used to carry out information acquisition, data processing and control of peripheral hardware circuits.

2.2 The overall block diagram of the system is as follows

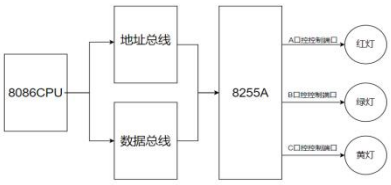

Figure 1: Overall System Block Diagram

2.3 The block diagram of the programme flow is as follows

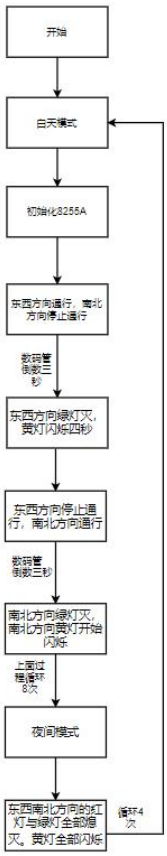

Figure 2: Overall block diagram of the programme flow

This course design using 8086CPU control 8255A control LED traffic lights. One of the decoder 74154 is equivalent to the role of the chip selector, because the course design only uses a piece of 8255A, will be connected to the IO1 port can be. At the same time 8255A should also be set according to the programme to light up the LED traffic lights.

3. SYSTEM HARDWARE PART DESIGN

3.1 Introduction to the Intel 8086 Microprocessor

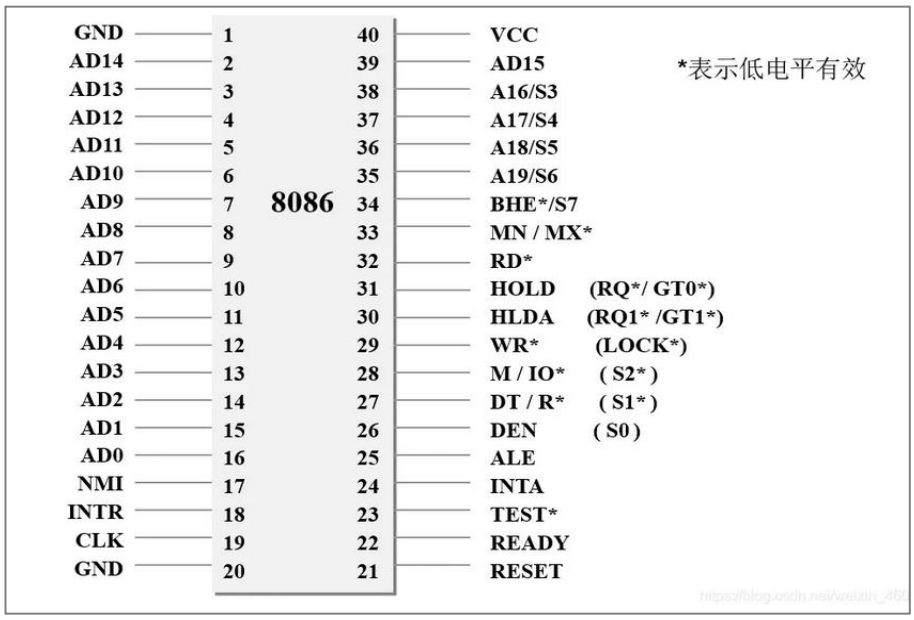

Figure 3: 8086 CPU pinout diagram

The Intel 8086 is a 16-bit microprocessor introduced by Intel in 1978. It is manufactured using the HMOS process, with 29,000 transistors on-chip, a single +5V power supply, a clock frequency of 4.77-10MHz, an on-chip data bus, registers, and an external data bus all of which are 16-bit, and a maximum addressable physical address of 1M.

To master the working performance and usage of a CPU, you should first understand its programming structure. In the programming structure of the 8086 CPU, functionally, divided into two parts, namely, the bus interface components (BIU) and the execution of components (EU). 8086's logical address is 20-bit, 16-bit physical address, for programmers, only need to consider the logical address can be 8086 for the 40-pin dual-row in-line package.

The Intel 8086 can operate in both maximum and minimum modes. Minimum and maximum modes are determined by whether the logic level connected to an MN/MN is a "1" or a "0".

In the minimalist approach, the microprocessor is used to form a small-scale uniprocessor system, where the microprocessor itself must provide all the control signals to the peripheral circuits. The microprocessor is used to form a larger scale multi-computer system. The signals in the minimal mode are as follows:

(1) AD15~AD0 (ADDRESS DATA BUS) Address/data multiplexing pin (bidirectional operation) Time-sharing multiplexed address/data lines.

(2) A19/S6~A16/S3 (Address/Status) outputs are time-multiplexed address/status lines. When used as an address line, A19~A16 together with A15~A0 constitute a 20-bit physical address for accessing memory.

(3) BHE/S7 (Bus High Enabale/Status) Bus High Byte Valid signal. Tri-state output, active low, used to indicate that the current data on the high 8-bit data line is valid.

(4) NMI (Non Maskable Interrupt Request) Non-maskable interrupt request signal. Triggered by external input, rising edge, not subject to the interrupt allow flag.

(5) INTR (Interrupt Request) Maskable interrupt request signal. It is input from external, level-triggered and active high.

(6) RD (Read) read signal. Tri-state output, active low, indicates that the CPU is currently reading memory or IO port.

(7) CLK (Clock) master clock pin (input). Input from the 8284 clock generator.The maximum clock frequency that can be used by the 8286 CPU varies with the chip model, 5MHz for the 8086, 10MHz for the 8086-1, and 8MHz for the 8086-2.

(8) RESET (reset) reset signal. Inputted externally and active high.

(9) READY (ready) Ready signal. Inputted externally and active high, it indicates that the memory or IO port accessed by the CPU is ready to transmit data.

(10) TEST test signal. When the CPU executes the WAIT instruction, it will test TEST every 5 clock cycles, if TEST is invalid, the CPU will be in the step-waiting state until TEST is valid, then the CPU will continue to execute the next instruction.

(11) MN/MX operating mode selection signal. When MN/MX is high, the CPU operates in minimum mode; when MN/MX is low, the CPU operates in maximum mode.

(12) GND/VCC power ground and power supply. the 8086 CPU requires only a single +5V power supply, fed from the VCC pin.

(13) INTA Interrupt response signal. Output to external, active low. During the interrupt response cycle, this signal indicates that the CPU responds to the INTR signal from the outside and is used as a selector signal for reading the interrupt type code.

(14) ALE Address latch allow signal. Output to external, active high. Used as a chip select signal for the address latch in minimal mode systems.

(15) DEN data allow signal, tri-state output, active low.

(16) DT/R Data Transmit/Receive control signal.

(17) M/IO memory/IO port access signals.

(18) WR Write Signal. Tri-state output, active low, indicates that the CPU is currently writing memory or IO port.

(19) HOLD bus request signal. Externally input, active high. Indicates that another processor/controller sharing the bus has requested the CPU to use the bus.

(20) HLDA Bus Request Response Signal. Output to external, active high.As soon as the CPU tests for a HOLD request, it makes HLDA active at the end of the current bus cycle to indicate that it is responding to this bus request and immediately cedes bus usage. The instruction execution components in the CPU can continue to operate without requesting the use of the bus.After HOLD becomes invalid, the CPU also invalidates HLDA and retracts the right to use the bus to continue operation.

3.2 Principle of operation of the 8255A chip

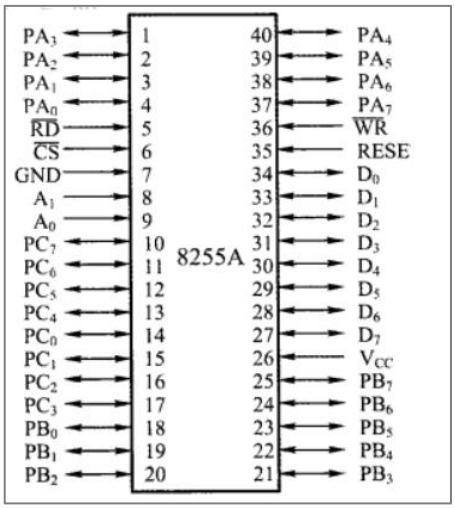

Figure 4: Programmable Peripheral Interface Circuit 8255A

The 8255 is a programmable parallel I/O interface chip from Intel with three 8-bit parallel I/O ports. Programmable parallel interface chip (40 pins) with 3 channels and 3 operating modes. The function of each port can be controlled by software The 8255 can be used as a microcontroller intermediate interface circuit when connecting with various peripherals.

The 8255, as the connection chip between the host and peripherals, must provide three bus interfaces , i.e. data lines, address line address line, and control line interfaces. At the same time must have and peripheral connection interface A, B, C port. As the 8255 programmable, so must have a logical control section, and thus the internal structure of the 8255 is divided into three parts: connected to the CPU part, connected to the peripheral part, the control part.

(1) Connection part with CPU

By definition, the 8255 is capable of transmitting 8-bit data in parallel, so its data lines are 8 D0 to D7. Since the 8255 has 3 channels A, B, and C, it only needs two address lines can address the A, B, and C ports and the control registers Therefore, the address lines In addition, the CPU has to read, write and chip select operation, so the control lines are chip select, reset, read and write signals. Each signal's pin The pin numbers of each signal are as follows:

① Data bus DB: Numbered D0 to D7, it is used to transfer 8-bit data between 8255 and CPU.

② Address bus AB: Numbered A0 to A1, it is used to select the A, B, and C ports with the control registers .

③ Control Bus CB: Chip select signal , Reset signal RST, write signal, read signal. When the CPU wants to perform read and write operations on the 8255, it must first send a Chip Selection signal to select the 8255 chip, and then send a read signal or write signal to read or write data to the 8255.

(2) Interface with Peripheral Interface Part

By definition, the 8255 has three channels A, B, and C with the peripheral connection, and each channel has 8 wires to connect with the peripheral, so the 8255 can be connected to the peripheral with 24 wires, and if switching control is performed, the 8255 can control 24 switches at the same time. Each channel's pin The pin numbers of each channel are as follows:

① Port A: Numbered PA0 to PA7, it is used to input and output 8-bit parallel data from 8255 to peripherals.

② Port B: Numbered PB0 to PB7, it is used to input and output 8-bit parallel data from 8255 to peripherals.

③ C port: numbered PC0 to PC7, used for 8255 to Peripheral Input and output 8-bit parallel data, when 8255 works in answer I/O mode, port C is used for answer signal communication.

(3) Controller section

The 8255 divides the three channels into two groups, i.e., PA0 to PA7 and PC4 to PC7 form Group A, and PB0 to PB7 and PC0 to PC3 form Group B. The controller is divided into two groups. As shown in Figure 7.5, the corresponding controllers are also divided into Group A controllers and Group B controllers, and the roles of the controllers in each group are as follows:

① Group A controller: Controls the input and output of the A and upper C ports.

② Group B controller: Controls the inputs and outputs of the B and lower C ports.

Pin Function:

RESET: Reset input line, when this input is at high level, all internal registers (including control registers) are cleared and all I/O ports are set to input mode.

CS: Chip select signal line, when this input CS: Chip select signal line, when this input pin When this input pin is low, i.e. /CS=0, it means the chip is selected, allowing the 8255 to communicate with the CPU; /CS=1, the 8255 can not do data transfer with the CPU.

RD: Read signal line, when this input RD: Read signal line, when this input pin is low, i.e., /RD generates a low pulse and /CS=0, the 8255 is allowed to read the data via the data bus The 8255 is allowed to send data or status information to the CPU through the data bus, i.e. the CPU reads information or data from the 8255.

WR: Write signal, when this input WR: Write signal, when this input pin is a low jump edge, i.e., /WR generates a low pulse and /CS=0, the CPU is allowed to write data or control words to the 8255.

D0 to D7: Tri-state bidirectional data bus D0 to D7: Tri-state bi-directional data bus, 8255 and CPU Data Transfer When the CPU executes input/output instructions, the 8-bit data read/write operation is realised through it, and the control word and status information are also transferred through the Data bus control words and status information are also transmitted through the data bus.

The 8255 has three mutually independent input/output channel ports, is powered by a single +5V power supply, and can operate in the following three ways.

Mode 0 - basic input/output mode; Mode 1 - selective input/output mode; Mode 2 - bidirectional selective input/output mode;

PA0 to PA7: Port A input and output lines, an 8-bit data output Latch / Buffer, one 8 - bit data input latch/buffer, an 8-bit data input latch/buffer, and an 8-bit data input latch The following are some examples. Works in any of three ways;

PB0 to PB7: Port B input and output lines, an 8-bit I/O Latch PB0 to PB7: Port B input/output lines, one 8 - bit I/O latch, one 8-bit I/O buffer. Cannot work in mode II;

PC0 to PC7: Port C input and output lines, an 8-bit data output Latch/ Buffer Port C can be divided into two 4-bit ports by the operation mode setting. Port C can be divided into two 4-bit ports by operation mode setting, and each 4-bit port contains a 4-bit Each 4-bit port contains a 4-bit latch/buffer Each 4-bit port contains a 4-bit latch, which can be used in conjunction with Port A and Port B respectively as a control signal output or status signal input. Each 4-bit port contains a 4-bit latch and can be used as a control signal output or status signal input in conjunction with ports A and B respectively. Cannot be operated in mode 1 or 2.

A1,A0: address selection lines, used to select the 8255's PA port, PB port, PC port and the control registers .

When A1=0,A0=0, PA port is selected.

When A1=0,A0=1, PB port is selected.

When A1=1,A0=0, PC port is selected.

When A1=1.A0=1, the control register is selected.

3.3 Digital tube working principle

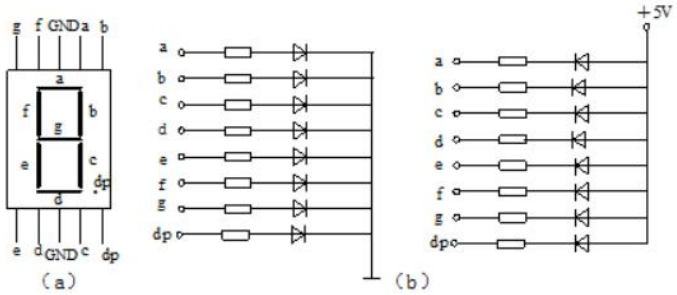

Figure 5: Structure of 8-segment digital tube

A digital tube, also known as a glow tube, is a device that displays numbers and other information. electronic device. The structure of its commonly used 8-segment digital tube is shown in Figure 3-6. The glass tube includes a wire mesh made of anode and several cathodes cathodes. Most digital tube cathodes are shaped like digits The cathode of most digital tubes is shaped like a number. The tube is filled with a low-pressure gas, usually mostly neon plus some mercury and/or argon . Charge one of the cathodes and the digital tube emits a coloured light, depending on the gas in the tube, usually orange or green.

Static Display Driver

Static drive is also known as DC drive. Static drive means that each segment code of each digital tube is driven by a microcontroller I/O port, or use BCD code binary-decimal decoder to drive. The advantage of static drive is simple programming, high display brightness, the disadvantage is that it occupies more I/O ports, such as driving 5 digital tube static display requires 5 × 8 = 40 I/O ports to drive, we must know that an 89S51 microcontroller available I/O ports only 32, the actual application must be added to the decoder driver to drive, increasing the complexity of the hardware circuit.

Dynamic Display Driver

Dynamic display interface is one of the most widely used display modes in microcontroller, the dynamic driver is to connect the 8 display strokes "a,b,c,d,e,f,g,dp" of all the digital tubes with the same name, and in addition to increase the bit-selective control circuit for the common pole COM of each digital tube, the bit-selective control is controlled by their own independent I/O lines, when the microcontroller outputs the glyph, all the digital tubes receive the same glyph, but which digital tube will display the glyph depends on the microcontroller's control of the bit-selective COM terminal circuit, so we just need to display the glyph of the desired digital tube, so we just have to control the bit-selective control of the desired digital tube, which is the same glyph. When the microcontroller output glyphs, all the digital tubes receive the same glyphs, but which digital tube will display the glyphs, depending on the microcontroller on the bit selective COM end of the circuit, so we just need to display the digital tube selective control is open, the bit will display the glyphs, there is no selective digital tube will not be bright. By controlling the COM terminal of each digital tube in turn, each digital tube is controlled to display in turn, which is the dynamic drive. In the process of rotating display, each digital tube is lit for 1 to 2ms, due to the human visual phenomenon and light-emitting diode afterglow effect. Afterglow effect Although the digital tubes are not lit at the same time, as long as the scanning speed is fast enough, the impression is a stable set of display data, there will be no sense of flicker, the effect of the dynamic display and static display is the same, to save a lot of I/O ports, and lower power consumption.

3.4 How LEDs work

LED's full name is Light Emitting Diode, meaning light-emitting diode, so essentially LED also belongs to a kind of diode, made of compounds containing gallium (Ga), arsenic (As), phosphorus (P), nitrogen (N), etc., take the ordinary diode, for example, when we give him a forward voltage, he will be able to conduction, and add a reverse voltage, then, this diode will be Cut off. This is because the core part of the light-emitting diode is composed of P-type semiconductor and N-type semiconductor wafer, in the P-type semiconductor and P-type semiconductor there is a transition layer between the semiconductor, known as the P-N junction, the N area has more free electrons, while the P area has more holes, when we add a forward voltage, the electrons will be attracted by the power plant and compounded with the holes, the free electrons and holes compounded with the release of heat, the LED lights. Principle and this diode is similar, but when the free electrons and holes are compounded, he releases light energy externally. In the development of microcontroller, we can use the high and low levels of the 8255 port to control the LED on and off.

4. SYSTEM CIRCUIT DIAGRAM DESIGN

4.1 8086 Traffic Simulation Diagram

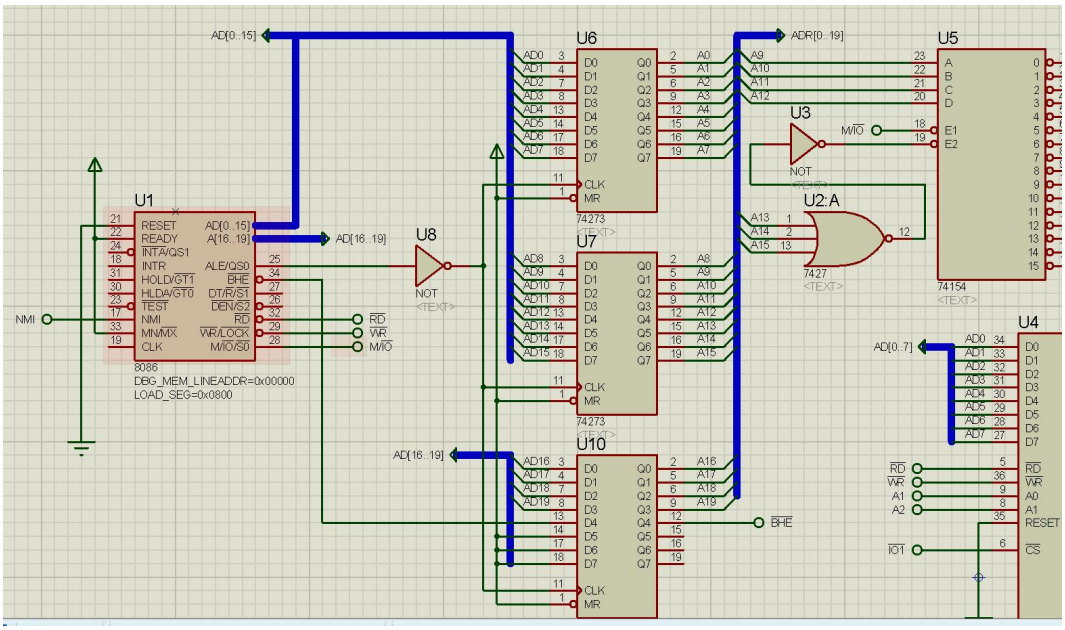

Figure 6: 8086 Control Circuit Diagram

Figure 6 is the 8086 control circuit, the circuit is the use of 8086 chip and 74273, 74154 chip to achieve data and address shared to the separation, through this circuit can be separated from the data line and the address line, where the data line can be the first 8255 control port to send data to reach the control of the 8255 chip. At the same time, the 74LS138 decoder we can select the signal to control the 8255A chip is selected, in order to determine the selected control chip. The use of the control circuit can greatly improve our development efficiency has been greatly improved, when the development of problems, we are also able to quickly identify the problem, and quickly solve the problem.

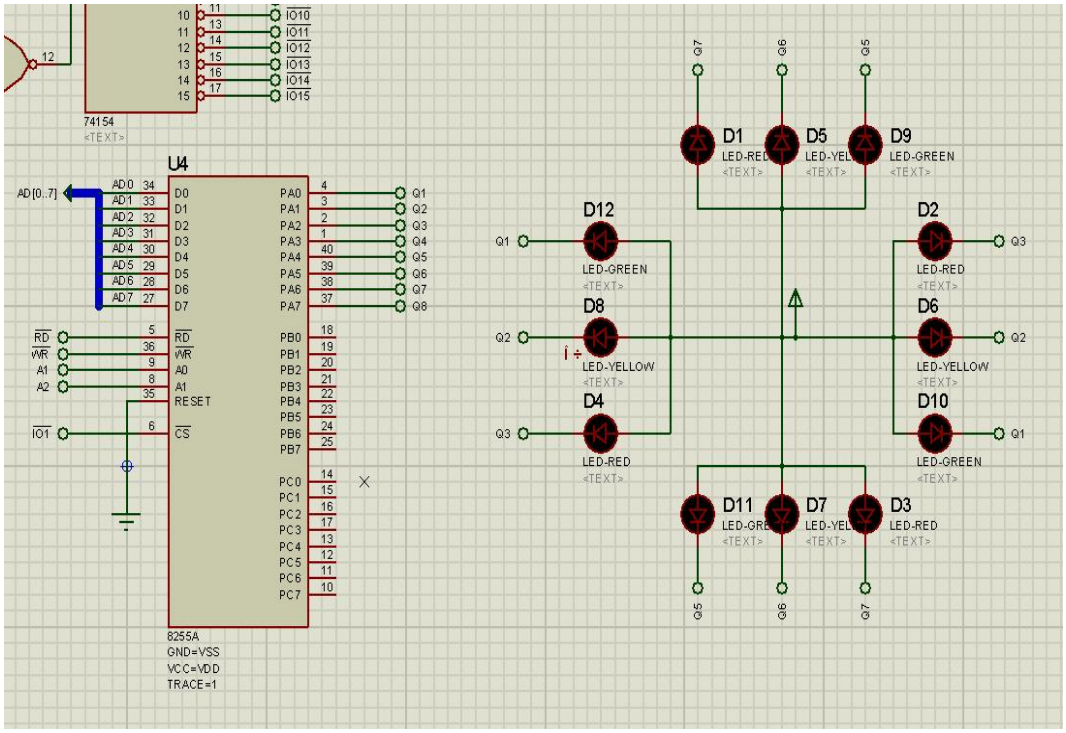

Figure 7: Traffic light part simulation

Figure 7 traffic light part of the simulation circuit is the use of 8255 control chip to achieve the function of traffic lights. When we use the peripheral circuit of the 8086 chip selected 8255A chip, elected 8255A control port using data transmission can control the flashing interval of the traffic lights and flashing time and other related parameters, for us to program quickly and efficiently.

4.2 Traffic Light Hardware Circuit Wiring Diagrams

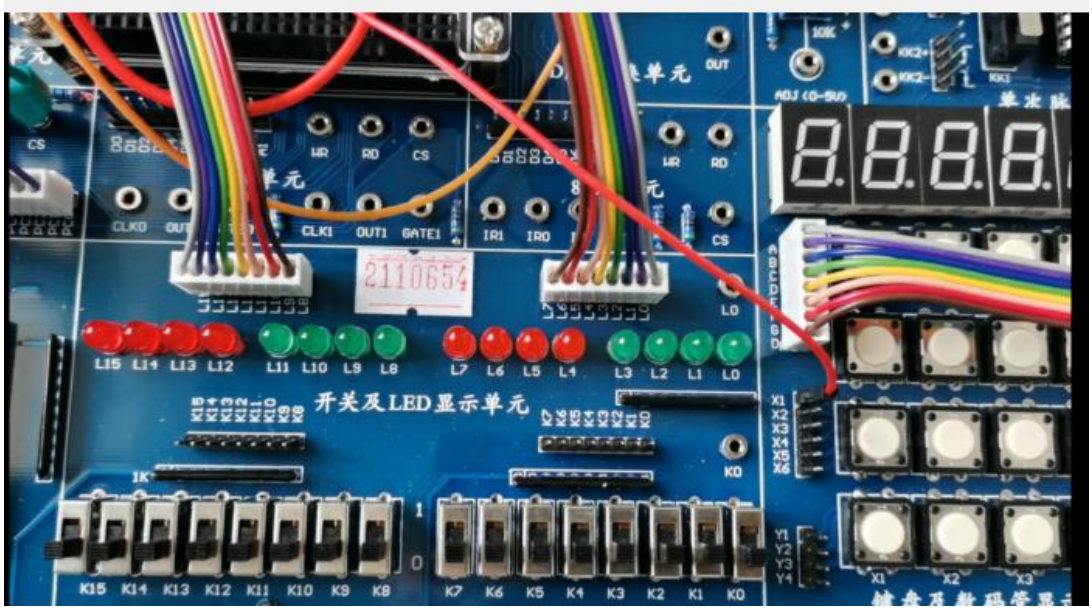

Figure 8: Hardware wiring diagram for traffic light section

The 8086 minimum system consists of an Intel 8086 microprocessor, a 74273 TTL with common clock reset octal D flip-flop, and a 74154 TTL 4-wire-16-wire decoder.

The 8086 has a 20-bit address line, where the high 4 bits A19-A16 are time-multiplexed with the status line S6-S3, and the low 16 bits AD15-AD0 are time-multiplexed with the data line. After the addresses are sent out at T1 of the

bus cycle, it is necessary to latch them with a latch so that the dead-bit address lines can be changed to status outputs at T2 and later, and the low 16-bit address lines should be used as data lines. In addition, indicating whether the eight-bit data line works, the data bus allow signal is time-sharing multiplexed with the status line S7, so it also needs to be latched. 21 lines need to use three pieces of 8-bit address latch, and here the 74273 is used. the I/O part of the connection to the peripheral hardware circuits consists of a 4-wire-16-wire decoder 74154, which is used to assign the I / O hardware address.

4.3 Peripheral Circuit for Controlling Traffic Light LEDs

As shown above, 12 LEDs are connected to the PA port of the 8255A, and the relative 3 LEDs are interfaced in reverse order. For the traffic lights of this circuit, low level can light up the LEDs, write different data can control different colours of LEDs to light up, to achieve the purpose of control.

8255A is designed for INTEL's microprocessor interface chip, 8255A is a programmable chip, can be set to change the working state of the programme, the CPU through which it is directly connected to the peripheral. 8255A the normal operation of each port needs to be written beforehand into the control registers of the control word that is, the initialisation of the 8255A programming.

The 8255A designed for this course works as follows:

Initialisation programming:

The 8255 works as follows

A mode 0, output, B mode 1, output.

The control word is 80H i.e. 1000 0000B, initialising the program:

MOV AL, 80H

OUT MY8255_MODE, AL

Where MY8255_MODE is the address of the 8255A mode control register.

4.4 Traffic light effect display

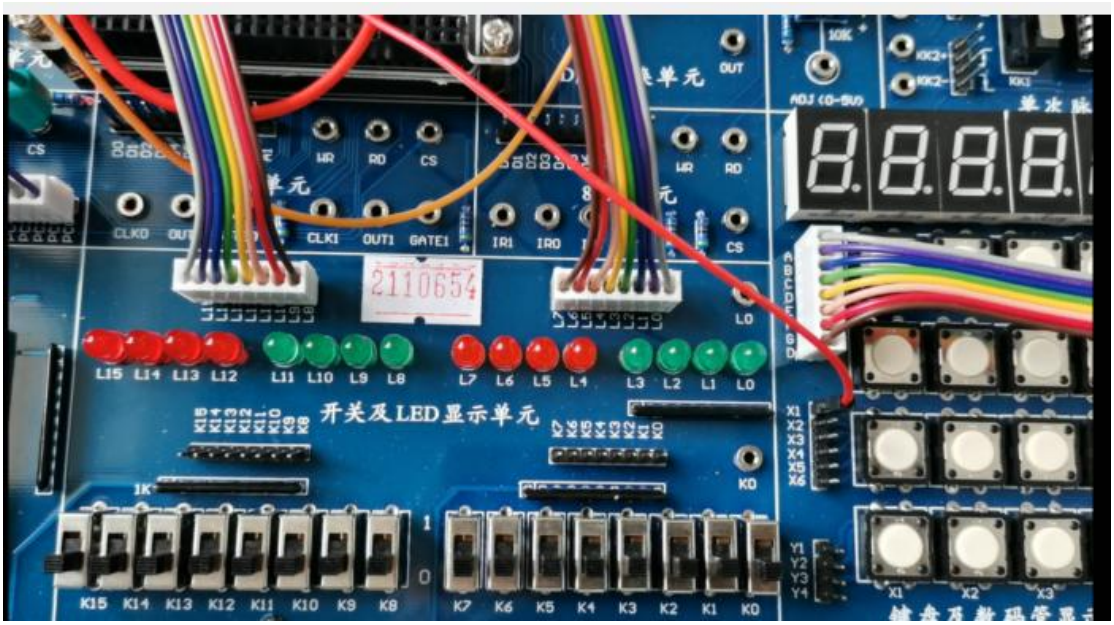

Figure 9: Hardware Connection Diagram of Traffic Light Section

Daylight mode:

Passing in the east-west direction and stopping in the north-south direction. That means the green light is on in the east-west direction and the red light is on in the north-south direction. At the same time, the digital tube starts counting down from 9-0 display.

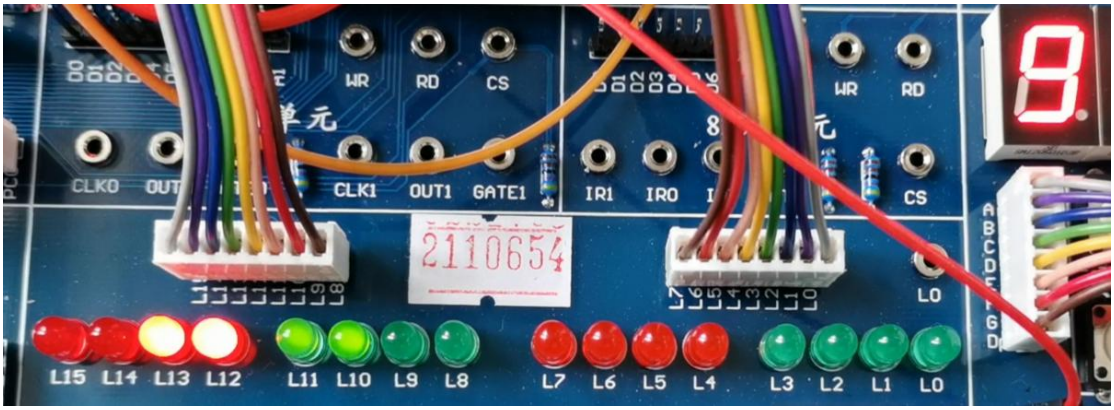

Figure 10: East-West Traffic, North-South Traffic Stopped

(2) Passage in the east-west direction, stop the passage in the north-south direction. When the digital tube number becomes 3, the green light in the east-west direction goes out, and the yellow light in the east-west direction starts to flash until the digital tube number shows 0, that is, the yellow light stops flashing.

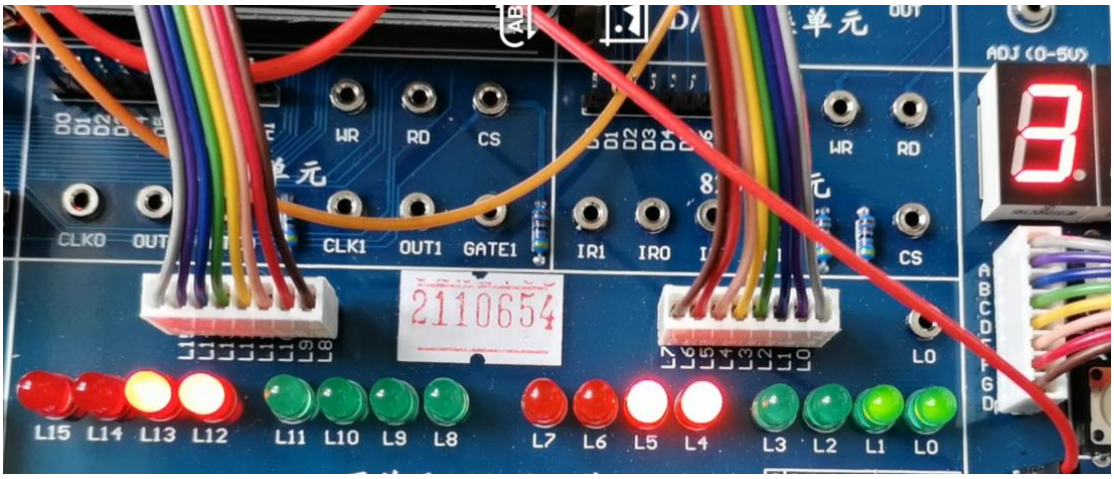

Figure 11: East-West Green Light Goes Out, East-West Yellow Light Starts Blinking

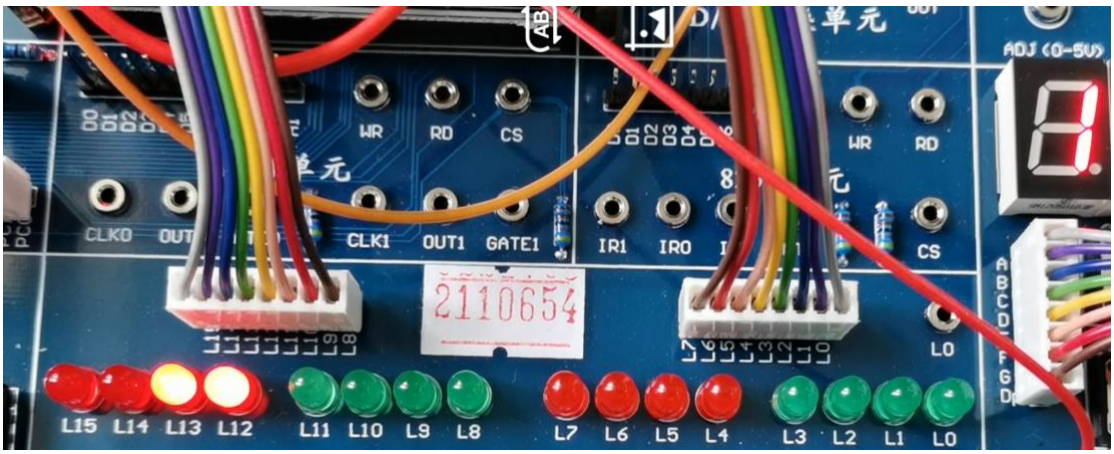

Figure 12: East-west green light goes out, east-west yellow light starts flashing

(3) Stop traffic in the east-west direction and pass in the north-south direction. That means the red light is on in the east-west direction and the green light is on in the north-south direction. At the same time, the digital tube starts counting down from 9-0 display.

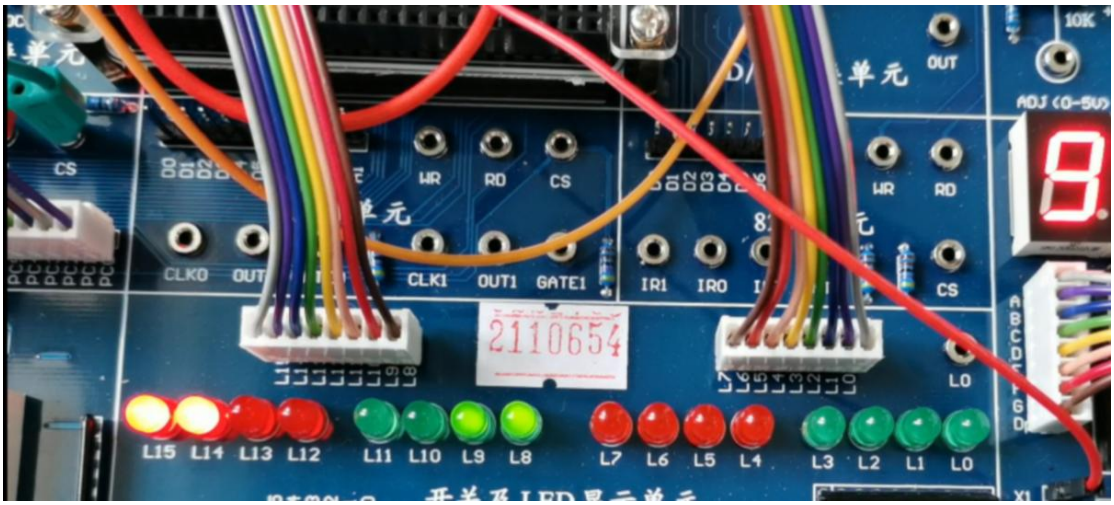

Figure 13: East-West Stopped, North-South Passing

(4) Stop passing in the east-west direction and pass in the north-south direction. When the digital tube number becomes 3, the green light in the north-south direction goes out, and the yellow light in the north-south direction starts to flash until the digital tube number shows 0, i.e. the yellow light stops flashing.

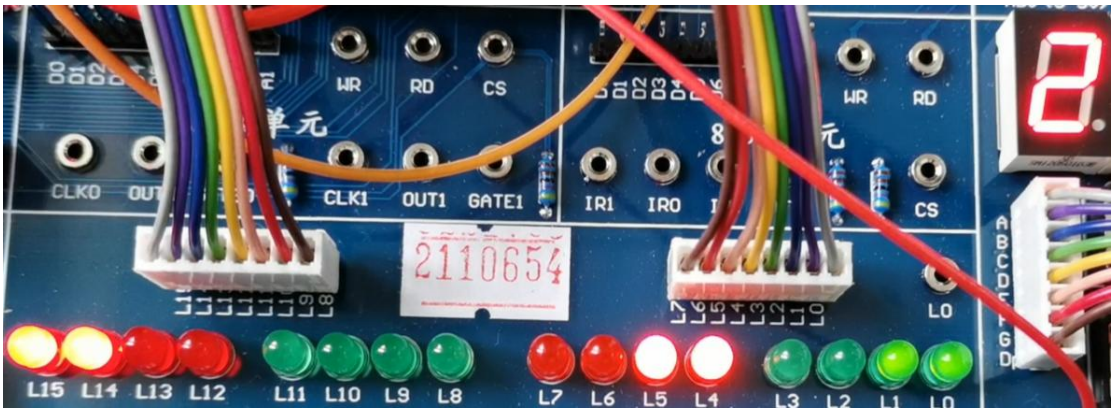

Figure 14: East-West Stopped, North-South Passing

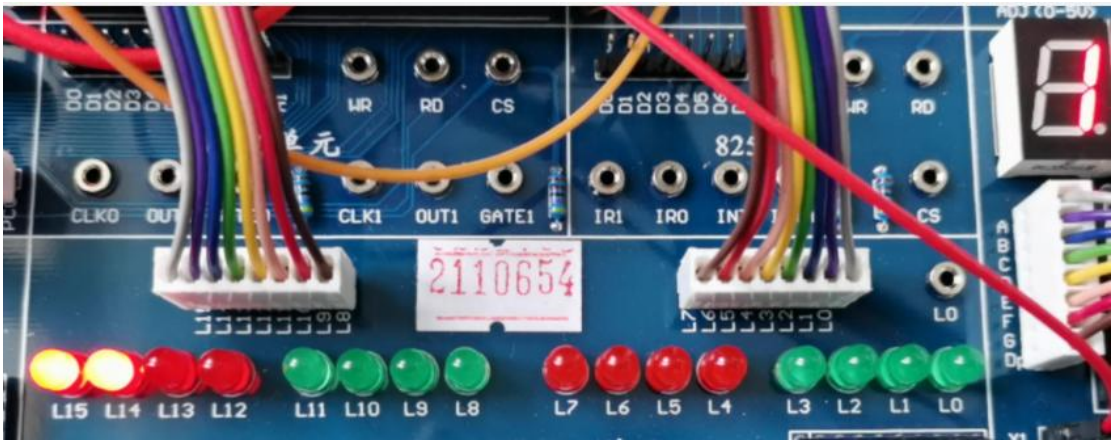

Figure 15: North-south direction green light goes out, north-south direction yellow light starts flashing

Night mode:

① The digital display turns off, and the red and green lights in the east-west and north-south directions all go out.

② All yellow lights in the east, west, south, and north directions flash at the same time.

③ Night Mode Cycle 4 times into Day Mode

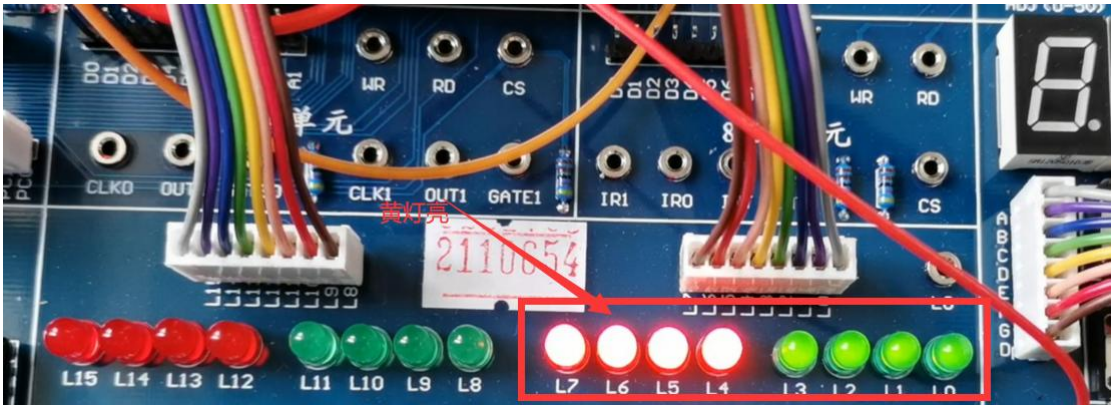

Figure 16: Four directions of the yellow light all on, southeast, northwest and green light off

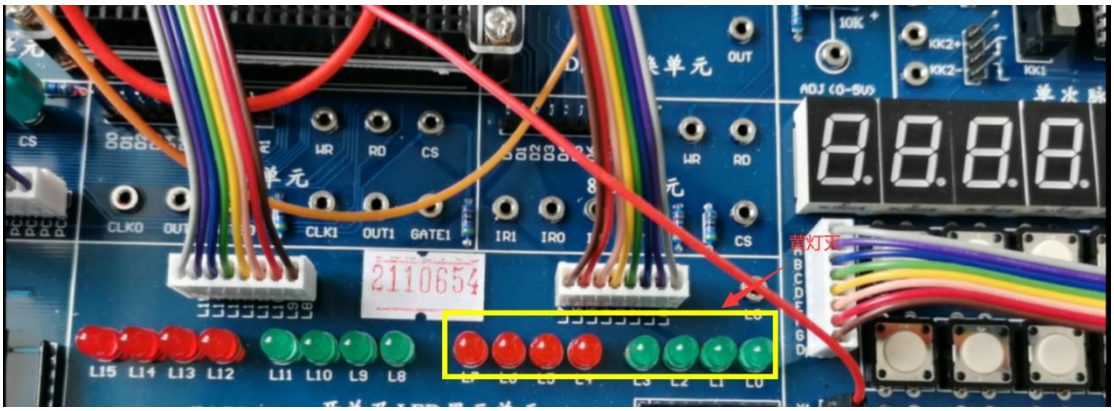

Figure 17: Four directions of the yellow light all on, southeast, northwest and green light off

5. ENVIRONMENTAL PROTECTION AND SUSTAINABLE DEVELOPMENT

With the development of the times, the pace of modern society is accelerated, more and more people for their own travelling and going to work convenience have purchased a car. In this case, the importance of traffic lights more and more prominent. A good, stable enough to run the traffic light control can make the whole city are running in an orderly manner, the car unimpeded on the road, not only saves everyone's time, but also saves the car running time, so that the carbon dioxide emissions build less, to protect our planet home.

The traffic light control we designed is a control system that can operate stably and play a certain role in protecting the environment, although it is not big, but it will also contribute to sustainable development.